Amendments to the Specification:

Please replace paragraph **[0011]** with the following re-written paragraph:

[0011] The following description provides method, system and apparatus for a flexible compression architecture utilizing internal cache residing in ~~mainmemory~~ main memory. In the following description, numerous specific details are set forth in order to provide a more thorough understanding of the present invention. It will be appreciated, however, by one skilled in the art that the invention may be practiced without such specific details. Those of ordinary skill in the art, with the included descriptions, will be able to implement appropriate logic circuits without undue experimentation.

Please replace paragraph **[0012]** with the following re-written paragraph:

[0012] As previously described, various problem exist for typical memory compression architectures. In contrast, in one aspect, the claimed subject matter utilizes a main memory for storing compression cache data. In another aspect, the claimed subject matter depicts a flexible compression architecture that may enable expansion of the compression cache by facilitating tag expansion. In yet another aspect, the claimed subject matter depicts a victim buffer and prioritization scheme for alleviating performance ~~impactsed~~ impacts by ~~of~~ compression and decompression operations.

Please replace paragraph **[0013]** with the following re-written paragraph:

[0013] Figure 1 illustrates an apparatus utilized in accordance with an embodiment. In one aspect and embodiment, the apparatus depicts a novel and flexible memory compression architecture that enables expansion of a compression cache by facilitating tag expansion. In yet another aspect, the apparatus depicts a victim buffer and prioritization scheme for alleviating performance impacts ~~association of~~ associated with compression and decompression operations. Furthermore, the apparatus depicts utilizing main memory for storing compression cache data.

Please replace paragraph **[0020]** with the following re-written paragraph:

[0020] Otherwise, in the event of a read miss, the pointer to the compressed memory location is obtained either from the CMPT cache 122 or from the CMPT 106 in main memory 104. . The CMPT stores the pointer (an address) to the compressed data that is being requested. In one embodiment, it will take one access to get this pointer and then another access to get the actual compressed data, a small cache in the memory interface is used to store the most recently used compressed data pointers. In one embodiment, the CMPT cache is first searched for the pointer. If this cache does not have the pointer, then the pointer is obtained from the main memory itself first. Then the location pointed to by the pointer is accessed subsequently to obtain the actual compressed memory data. ~~The~~

Please replace paragraph **[0021]** with the following re-written paragraph:

[0021] ~~Subsequently, After the pointer is obtained, .~~ Consequently, the compressed memory location designated by the pointer is accessed and the data is forwarded to the decompression engine 128. Subsequently, the decompressed data is output from the

decompression engine 128 and is forwarded to the requester of the initial memory access of the incoming address. Likewise, in one embodiment the decompressed data is subsequently written to the compression engine cache in order to store the most recently accessed memory item in uncompressed form. Before ~~doing~~ this, a victim data from the compression cache is chosen and vacated to the victim buffer.. In the event of a compression cache write miss, the data is compressed by the compression engine and is stored in the compressed memory location based at least in part on a pointer that may be indicated by a CMPT cache entry. Otherwise, if the pointer is not available in the CMPT cache, then a corresponding CMP table entry in the main memory 104 is accessed by using a CMPT offset calculator 124.

Please replace the abstract with the following:

~~Method, systems and apparatus for a flexible compression architecture utilizing internal cache residing in main memory circuits.~~ A flexible compression architecture with a main memory for storing compression cache data that enables expansion of the compression cache by facilitating tag expansion by utilizing a victim buffer and prioritization scheme for alleviating performance impacts by compression and decompression operations.